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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

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1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 23] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention PLUS TITLE PAGE
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets 4] (Figs. 1-8)
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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SEMICONDUCTOR PROCESSING METHODS

* * * * *

INVENTORS

Weimin Li
John Q. Li

ATTORNEY'S DOCKET NO. MI22-1035

SEMICONDUCTOR PROCESSING METHODS

TECHNICAL FIELD

The invention pertains to semiconductor processing methods, and particularly pertains to methods of removing some portions of a layer from over a semiconductive substrate, while leaving other portions of the layer remaining over the substrate.

BACKGROUND OF THE INVENTION

Modern semiconductor processing frequently involves photolithographic methods to pattern materials into very small structures, which are ultimately incorporated into a semiconductor circuit. An exemplary prior art method for forming small structures from a layer of material is as follows. First, the layer of material is provided over a semiconductive substrate. Subsequently, a layer of photoresist is provided over the layer of material. A photolithographic mask is then provided over the layer of photoresist and light is shined through the mask to expose portions of the layer of photoresist while leaving other portions unexposed. The photoresist typically comprises an unsaturated organic material, such as, for example, a material comprising one or more unsaturated carbon-containing rings. The exposed portions are rendered either more or less soluble in a solvent relative to the unexposed portions. If the exposed portions are rendered more soluble,

the resist is referred to as a positive photoresist (as a positive image of a pattern from the photolithographic mask is transferred to the photoresist), and if the exposed portions are rendered less soluble, the photoresist is referred to as a negative photoresist (as a negative image of the pattern from the photolithographic mask is transferred to the photoresist). In any event, the photoresist is exposed to a solvent and either the exposed or unexposed portions are removed while leaving the other of the exposed or unexposed portions remaining over the layer of material. Such patterns the photoresist into a patterned mask overlaying the layer of material. The layer of material is then exposed to conditions which transfer a pattern from the patterned mask to the layer of material (i.e., which removes portions of the layer of material not covered by photoresist, while leaving the portions of the layer material that are covered by photoresist). Subsequently, the photoresist is removed and the substrate having the patterned layer of material thereon is subjected to subsequent processing steps to form an integrated circuit over the substrate.

Typically, the semiconductive substrate referred to above is in the form of a wafer and a plurality of semiconductor packages (i.e., individual integrated circuits) are simultaneously formed over the wafer. After the formation of the plurality of semiconductor packages is complete, the wafer is subjected to a die-cutting process to separate the individual integrated circuits from one another. In wafer fabrication

processes employed to date, photoresist is entirely removed from a wafer prior to subjecting the wafer to a die-cutting process. Among the reasons for removal of the photoresist is that the photoresist is not a material suitable for incorporation into semiconductor circuits. It would be desirable to develop alternative methods for patterning structures during semiconductor circuit fabrication processes.

In an area of semiconductor processing considered to be unrelated to the above-described photolithographic processing methods, a recently developed technique for forming insulative materials is Flowfill™ Technology, which has been developed by Trikon Technology of Bristol, U.K. The process can be utilized for forming either silicon dioxide or methylsilicon oxide ($(CH_3)_xSiO_{2-x}$), for example. The process for forming silicon dioxide is as follows. First, SiH_4 and H_2O_2 are separately introduced into a chemical vapor deposition (CVD) chamber, such as a parallel plate reaction chamber. The reaction rate between SiH_4 and H_2O_2 can be moderated by the introduction of nitrogen into the reaction chamber. A semiconductive wafer is provided within the chamber, and ideally maintained at a suitably low temperature, such as 0°C, at an exemplary pressure of 1 Torr to achieve formation of a silanol-type structure of the formula $Si(OH)_x$, which is predominantly $Si(OH)_4$. The $Si(OH)_4$ condenses onto the wafer surface. Although the reaction occurs in the gas phase, the deposited $Si(OH)_4$ is in the form of a viscous liquid which flows to fill small gaps on the wafer surface. In

applications where deposition thickness increases, surface tension drives the deposited layer flat, thus forming a planarized layer over the substrate.

The liquid $Si(OH)_4$ is typically converted to a silicon dioxide structure by a two-step process. First, planarization of the liquid film is promoted by increasing the temperature to above 100°C, while maintaining the pressure of about 1 Torr, to result in solidification and formation of a polymer layer. Thereafter, the temperature is raised to above 400°C, while maintaining the pressure of greater than 1 Torr, to form SiO_2. The processing above 400°C also provides the advantage of driving undesired water from the resultant SiO_2 layer.

The formation of methylsilicon oxide is accomplished similarly to that described above for forming silicon dioxide, with the exception that methylsilane ($(CH_3)_zSiH_{4-z}$, wherein z is at least 1 and no greater than 4) is combined with the hydrogen peroxide to produce a methylsilanol, instead of combining the silane (SiH_4) with the hydrogen peroxide to form silanol.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a semiconductor processing method wherein a layer of material is formed over a semiconductive wafer substrate. Some portions of the layer are exposed to energy while other portions are not exposed. The exposure to

energy alters physical properties of the exposed portions relative to the unexposed portions. After the portions are exposed, the exposed and unexposed portions of the layer are subjected to common conditions. The common conditions are effective to remove the material and comprise a rate of removal that is influenced by the altered physical properties of the layer. The common conditions remove either the exposed or unexposed portions faster than the other of the exposed and unexposed portions. After the selective removal of the exposed or unexposed portions, and while the other of the exposed and unexposed portions remains over the substrate, the wafer is cut into separated die.

In another aspect, the invention encompasses another semiconductor processing method. A layer of $(CH_3)_ySi(OH)_{4-y}$ is formed over a substrate, wherein y is greater than 0 and less than 4. Some portions of the layer are exposed to ultraviolet light while other portions are not exposed. The exposure to ultraviolet light converts the exposed portions to $(CH_3)_xSiO_{2-x}$, wherein x is greater than 0 and less than 2. After the exposure to ultraviolet light, the exposed and unexposed portions of the layer are subjected to hydrofluoric acid to selectively remove the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative to the $(CH_3)_xSiO_{2-x}$ of the exposed portions.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a first step of a processing method in accordance with the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a step subsequent to that of Fig. 2 in accordance with a first embodiment processing method of the present invention.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment shown at a step subsequent to that of Fig. 2, and in accordance with a second embodiment processing sequence of the present invention.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that of Fig. 5.

Fig. 7 is a top view of a semiconductive wafer, such as the wafer incorporating the fragment of Fig. 1, shown prior to subjecting the wafer to a die-cutting process.

Fig. 8 is a top view of portions of the Fig. 7 semiconductive wafer shown after the wafer is subjected to a die-cutting process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention encompasses methods for utilizing energy to form patterned masking materials on a wafer. In particular aspects of the invention, the patterned masking materials are retained on a wafer after a die-cutting process. In other particular aspects of the invention, the patterned masking materials comprise silicon. The invention is described with reference to a preferred embodiment in Figs. 1-8.

Referring to Fig. 1, a semiconductive wafer fragment 10 is illustrated at a preliminary step of a processing sequence encompassed by the present invention. Wafer fragment 10 comprises a semiconductive substrate 12. Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with a p-type conductivity enhancing dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure,

including, but not limited to, the semiconductive substrates described above.

A first layer of material 14 is formed over substrate 12, and a second layer of material 16 is formed over first layer 14. The material of first layer 14 can be either a conductive material or an insulative material, and is not particularly germane to the present invention. The material of second layer 16 has physical properties which can be altered by exposure to energy. The material of second layer 16 can comprise, for example, methylsilanol ($(CH_3)_ySi(OH)_{4-y}$) or silanol ($Si(OH)_4$, either of which can be formed by methods described above in the "Background" section of this disclosure. Both methylsilanol and silanol have physical properties which can be altered by exposure to, for example, electron beam energy, ultraviolet light or plasma. For instance, if portions of either silanol or methylsilanol are exposed to ultraviolet light, such portions will have a higher etch rate in hydrofluoric acid than will portions not exposed to the ultraviolet light. The exposure of methylsilanol to ultraviolet light converts it to the insulative material $(CH_3)_xSiO_{2-x}$, and exposure of silanol to ultraviolet light converts it silicon dioxide.

Referring to Fig. 2, an energy source 18 is provided over wafer fragment 10, and a patterned photolithographic mask 20 is provided between source 18 and second layer 16. Mask 20 comprises orifices 22 extending therethrough. In operation, energy 24 is emitted from

source 18 and toward mask 20. In the illustrated embodiment, the energy is shown as light waves which can comprise, for example, wavelengths corresponding to ultraviolet light. Mask 20 blocks some of the light waves, while other light waves penetrate through orifices 22 to reach layer 16. Layer 16 is thus divided into portions 30 which are exposed to the radiation from source 18 and portions 32 which are shielded by mask 20 and not exposed to radiation 24. The exposure of layer 16 to radiation 24 alters physical properties of the material of layer 16 within exposed regions 30 relative to physical properties of the material in unexposed portions 32.

After the exposure to radiation 24, the exposed portions 30 and unexposed portions 32 of layer 16 are exposed to common conditions which are effective to remove the material of layer 16. Further, the common conditions comprise a rate of removal of the material of layer 16 that is influenced by physical properties altered by exposure to radiation 24. Accordingly, exposed portions 30 are removed at a different rate than unexposed portions 32. Figs. 3 and 4 illustrate an embodiment wherein exposed portions 30 are removed at a slower rate than unexposed portions 32, and Figs. 5 and 6 illustrate an embodiment wherein the exposed portions are removed at a faster rate than the unexposed portions.

Referring first to the embodiment of Figs. 3 and 4, and specifically referring to Fig. 3, substrate 10 is illustrated after exposure

to conditions which remove exposed portions 32 (Fig. 2) more rapidly than unexposed portions 30, to leave only unexposed portions 30 remaining over first material 14. In an exemplary embodiment, the material of layer 16 can comprise either methylsilanol or silanol, the radiation 24 (Fig. 2) can comprise ultraviolet light, and the common conditions can comprise exposure to hydrofluoric acid. The ultraviolet light converts exposed material of layer 16 to either methylsilicon dioxide or silicon dioxide, and thus renders such exposed portions more resistant to hydrofluoric acid removal than unexposed portions comprising either methylsilanol or silanol. In the exemplary embodiment, it is found that the portions of a methylsilanol or silanol layer 16 exposed to ultraviolet light are removed by hydrofluoric acid at a rate that is at least about 5 times slower than portions of layer 16 not exposed to ultraviolet light. The portions not exposed to ultraviolet light can thus be selectively removed relative to the portions that have been exposed to ultraviolet light. For purposes of interpreting this disclosure and the claims that follow, a first material is "selectively removed" relative to another material if the first material is removed at a rate that is at least 3 times faster than a rate at which the other material is removed.

Referring to Fig. 4, a pattern is transferred from exposed portions 30 to underlying layer 14. Specifically, portions of layer 14 are removed by an etch. The conditions of the etch will vary depending

on the material of layer 14, and can comprise conventional methods which will be recognized by persons of ordinary skill in the art for utilization with various materials of layer 14.

Referring to 5 and 6, processing similar to that of Figs. 3 and 4 is illustrated with the exception that it is exposed portions 30 (Fig. 2) that have a faster rate of removal than unexposed portions 32 when layer 16 is subjected to conditions for removing the material of layer 16.

An advantage of the present invention relative to prior art methods described above in the "Background" section of this disclosure is that the photolithographically patterned layer 16 does not comprise photoresist. Accordingly, layer 16 can have attributes desired in structures formed over substrate 12. For instance, in the above-described exemplary embodiment of Figs. 3 and 4, the remaining portions 30 of layer 16 comprise an insulative material (either silicon dioxide or methylsilicon oxide). Such insulative material can be utilized for separating conductive components of a semiconductor circuit from one another. In some applications, the methylsilicon oxide can be more preferred than the silicon dioxide, as methylsilicon oxide has a lower dielectric constant than silicon oxide. Accordingly, methylsilicon oxide can reduce parasitic capacitance between adjacent conductive components relative to silicon dioxide. The advantages of utilizing methylsilicon oxide can be generally realized from silicon oxides having the generic

formula R-Si-O, wherein R is an organic group. R can comprise, for example, a hydrocarbon group.

Figs. 7 and 8 illustrate subsequent processing which can occur after the processing of either Figs. 3 and 4, or the processing of Figs. 5 and 6. Specifically, Fig. 7 is a view of an entirety of a semiconductive wafer 50 which has been processed. The semiconductive wafer has a plurality of semiconductor structures (e.g., circuitry) formed thereover (not shown) and is subdivided into circuit packages 52 (only some of which are labeled). Imaginary dashed lines 53 are provided to show boundaries between adjacent semiconductor circuit packages 52. For reasons discussed above, structures comprised by packages 52 can comprise portions of photolithographically patterned layer 16 incorporated therein.

Referring to Fig. 8, wafer fragment 50 (Fig. 7) is illustrated after being subjected to a die-cutting process, wherein the wafer has been cut into separated die corresponding to packages 52.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or

modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A semiconductor processing method, comprising:

forming a layer of material over a semiconductive wafer substrate;

exposing some portions of the layer to energy while leaving other portions unexposed, the exposing altering physical properties of the exposed portions of material relative to the unexposed portions of material;

after the exposing, subjecting the exposed and unexposed portions of the layer to common conditions, the common conditions being effective to remove the material and comprising a rate of removal that is influenced by the altered physical properties of the layer, the common conditions removing either the exposed or unexposed portions faster than the other of the exposed and unexposed portions; and

after the selective removal of the exposed or unexposed portions, and while the other of the exposed and unexposed portions remains over the substrate, cutting the wafer into separated die.

2. The method of claim 1 wherein material comprises silicon.

3. The method of claim 1 wherein the material comprises carbon, silicon and oxygen.

4. The method of claim 1 wherein the material comprises silicon bound to a hydrocarbon group and bound to oxygen.

5. The method of claim 1 wherein the material comprises $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less than 4.

6. The method of claim 1 wherein the material comprises $Si(OH)_4$.

7. The method of claim 1 wherein the energy is in the form of ultraviolet light.

8. The method of claim 1 wherein the energy is in the form of an electron beam.

9. The method of claim 1 wherein the energy is in the form of a plasma.

10. A semiconductor processing method, comprising:

forming a layer of a silicon-comprising material over a substrate;

exposing some portions of the layer to energy while leaving other portions unexposed, the exposing altering physical properties of the exposed portions relative to the unexposed portions; and

after the exposing, subjecting the exposed and unexposed portions of the layer to common conditions, the common conditions being effective to remove the silicon-comprising material and comprising a rate of removal that is influenced by the altered physical properties of the layer, the common conditions removing either the exposed or unexposed portions faster than the other of the exposed and unexposed portions.

11. The method of claim 10 wherein the silicon-comprising material comprises carbon, silicon and oxygen.

12. The method of claim 10 wherein the silicon-comprising material comprises silicon bound to a hydrocarbon group and bound to oxygen.

13. The method of claim 10 wherein the silicon-comprising material comprises silicon bound to a hydrocarbon group and bound to oxygen, and wherein the hydrocarbon group does not comprise a carbon-containing ring.

14. The method of claim 10 wherein the silicon-comprising material comprises $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less than 4.

15. The method of claim 10 wherein the silicon-comprising material comprises $Si(OH)_4$.

16. The method of claim 10 wherein the energy is in the form of ultraviolet light.

17. The method of claim 10 wherein the energy is in the form of an electron beam.

18. The method of claim 10 wherein the energy is in the form of a plasma.

19. The method of claim 10 wherein the silicon-comprising material comprises $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less than 4, and the energy is in the form of ultraviolet light; and wherein:

the exposing comprises passing the ultraviolet light through openings in a patterned mask and onto the layer of material to expose said some portions of the layer to the ultraviolet light while leaving said other portions unexposed; and

the common conditions comprising subjecting the entire layer to hydrofluoric acid, the hydrofluoric acid removing portions of the layer that were not exposed to ultraviolet light at a faster rate than portions of the layer that were exposed to ultraviolet light.

20. The method of claim 10 wherein the silicon-comprising material comprises $Si(OH)_4$ and the energy is in the form of ultraviolet light; and wherein:

the exposing comprises passing the ultraviolet light through openings in a patterned mask and onto the layer of material to expose said some portions of the layer to the ultraviolet light while leaving said other portions unexposed; and

the common conditions comprising subjecting the entire layer to a solvent comprising hydrofluoric acid, the hydrofluoric acid removing portions of the layer that were not exposed to ultraviolet light at a faster rate than portions of the layer that were exposed to ultraviolet light.

21. The method of claim 10 wherein the silicon-comprising material comprises $Si(OH)_4$ and the energy is in the form of an electron beam; and wherein:

the exposing comprises exposing said some portions of the layer to the electron beam while leaving said other portions unexposed; and

the common conditions comprising subjecting the entire layer to hydrofluoric acid, the hydrofluoric acid removing portions of the layer that were not exposed to the electron beam at a faster rate than portions of the layer that were exposed to the electron beam.

22. A semiconductor processing method, comprising:

forming a layer of $(CH_3)_ySi(OH)_{4-y}$, with y being greater than 0 and less than 4, over a substrate;

exposing some portions of the layer to ultraviolet light while leaving other portions unexposed, the exposing converting the exposed portions to $(CH_3)_xSiO_{2-x}$, with x being greater than 0 and less than 2; and

after the exposing, subjecting the exposed and unexposed portions of the layer to hydrofluoric acid to selectively remove the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative to the $(CH_3)_xSiO_{2-x}$ of the exposed portions.

23. The method of claim 22 wherein the ultraviolet light is passed onto the layer of $(CH_3)_ySi(OH)_{4-y}$ through openings in a patterned mask.

24. The method of claim 22 wherein the substrate is a semiconductive wafer, and further comprising:

after the selective removal of the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions, and while the $(CH_3)_xSiO_{2-x}$ of the exposed portions remains over the substrate, cutting the wafer into separated die.

25. A semiconductor processing method, comprising:

forming a layer of $Si(OH)_4$ over a substrate;

exposing some portions of the layer to energy while leaving other portions unexposed, the exposing converting the exposed portions to SiO_2; and

after the exposing, subjecting the exposed and unexposed portions of the layer to hydrofluoric acid to selectively remove the $Si(OH)_4$ of the unexposed portions relative to the SiO_2 of the exposed portions.

26. The method of claim 25 wherein the energy is in the form of ultraviolet light.

27. The method of claim 25 wherein the energy is in the form of ultraviolet light and is passed onto the layer of $Si(OH)_4$ through openings in a patterned mask.

28. The method of claim 25 wherein the energy is in the form of an electron beam.

29. The method of claim 25 wherein the substrate is a semiconductive wafer, and further comprising:

after the selective removal of the $Si(OH)_4$ of the unexposed portions, and while the SiO_2 of the exposed portions remains over the substrate, cutting the wafer into separated die.

ABSTRACT OF THE DISCLOSURE

In one aspect, the invention encompasses a semiconductor processing method. A layer of material is formed over a semiconductive wafer substrate. Some portions of the layer are exposed to energy while other portions are not exposed. The exposure to energy alters physical properties of the exposed portions relative to the unexposed portions. After the portions are exposed, the exposed and unexposed portions of the layer are subjected to common conditions. The common conditions are effective to remove the material and comprise a rate of removal that is influenced by the altered physical properties of the layer. The common conditions remove either the exposed or unexposed portions faster than the other of the exposed and unexposed portions. After the selective removal of the exposed or unexposed portions, and while the other of the exposed and unexposed portions remains over the substrate, the wafer is cut into separated die. In another aspect, the invention encompasses another semiconductor processing method. A layer of $(CH_3)_ySi(OH)_{4-y}$ is formed over a substrate. Some portions of the layer are exposed to ultraviolet light while other portions are not exposed. The exposure to ultraviolet light converts the exposed portions to $(CH_3)_xSiO_{2-x}$. After the exposure to ultraviolet light, the exposed and unexposed portions of the layer are subjected to hydrofluoric acid to selectively remove the $(CH_3)_ySi(OH)_{4-y}$ of the unexposed portions relative to the $(CH_3)_xSiO_{2-x}$ of the exposed portions.

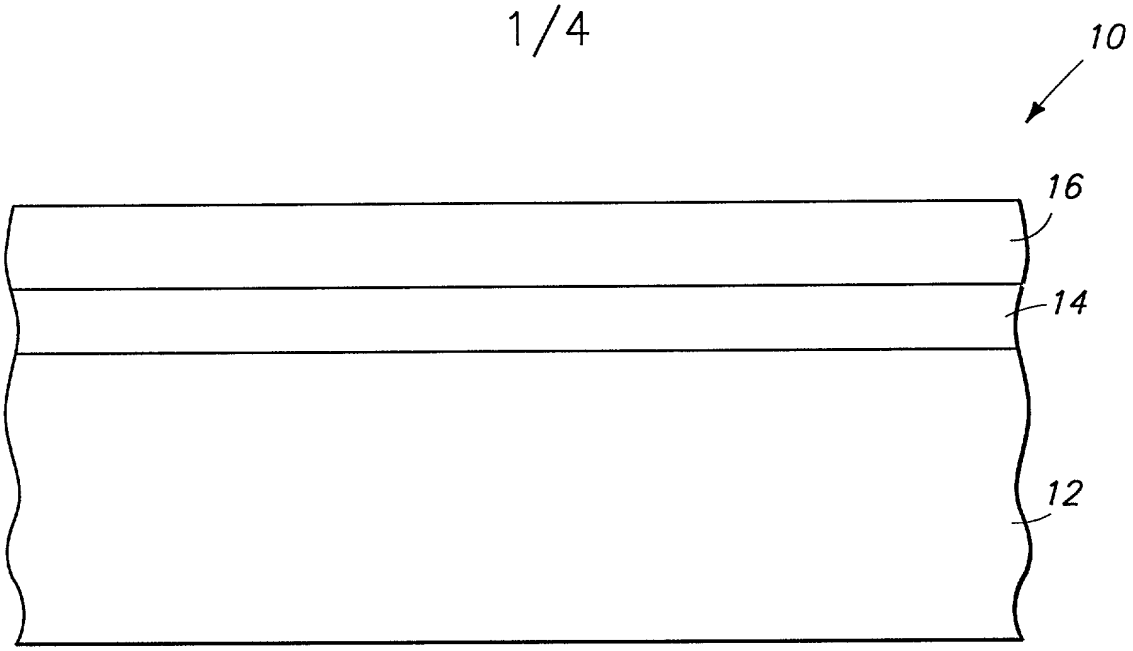

Fig. 1

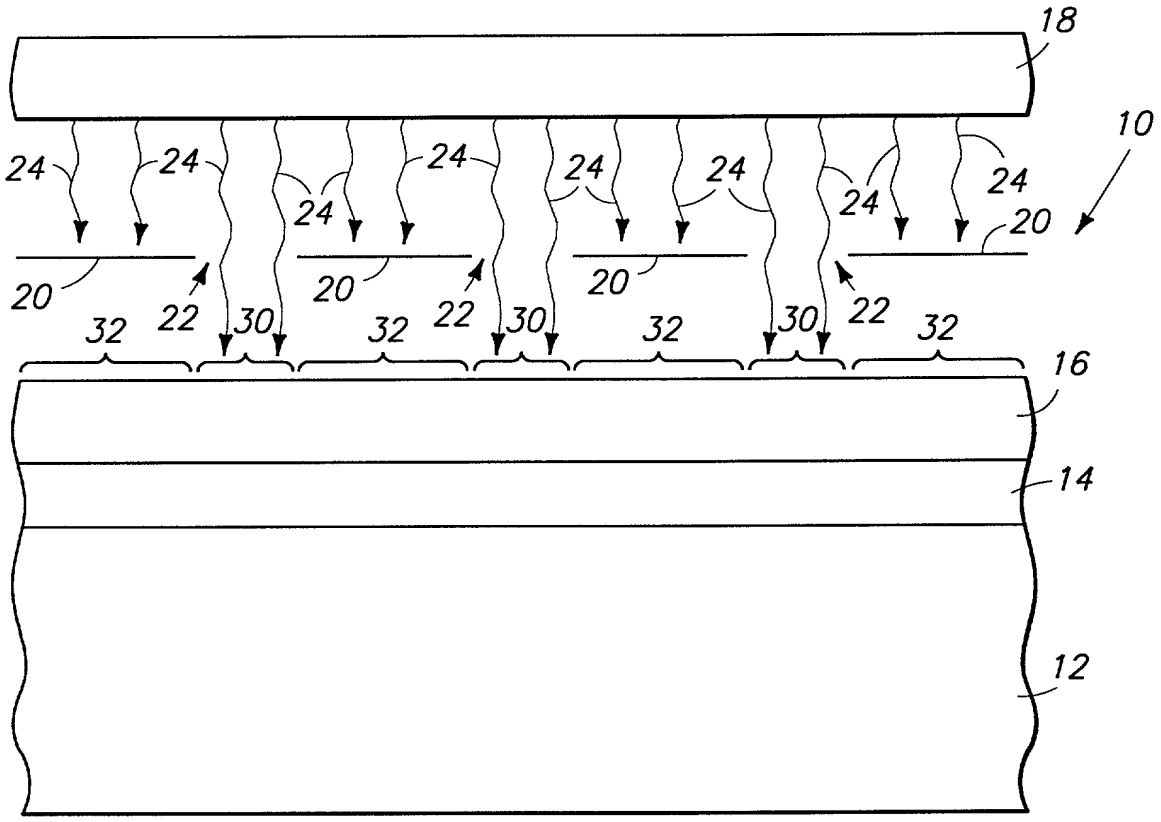

Fig. 2

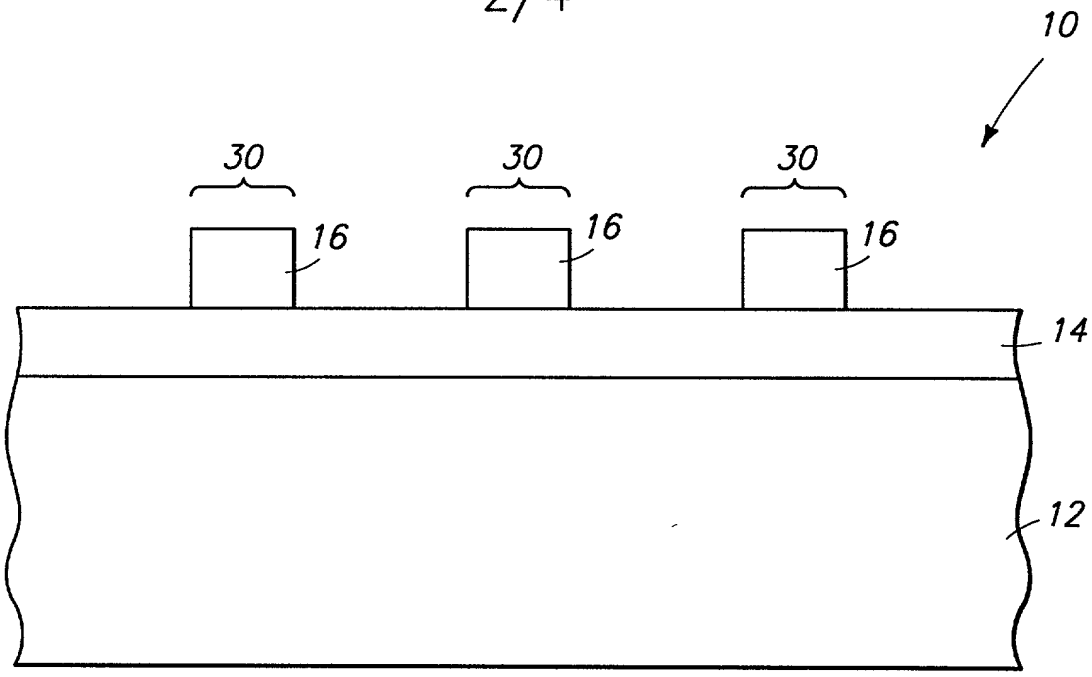

Fig 3

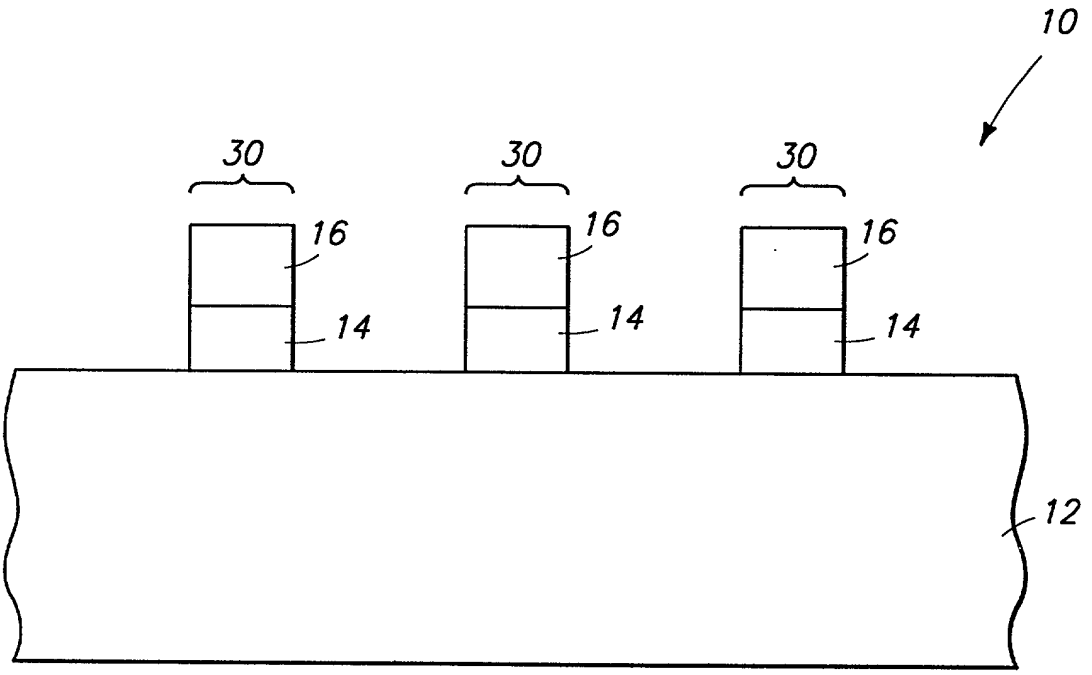

Fig 4

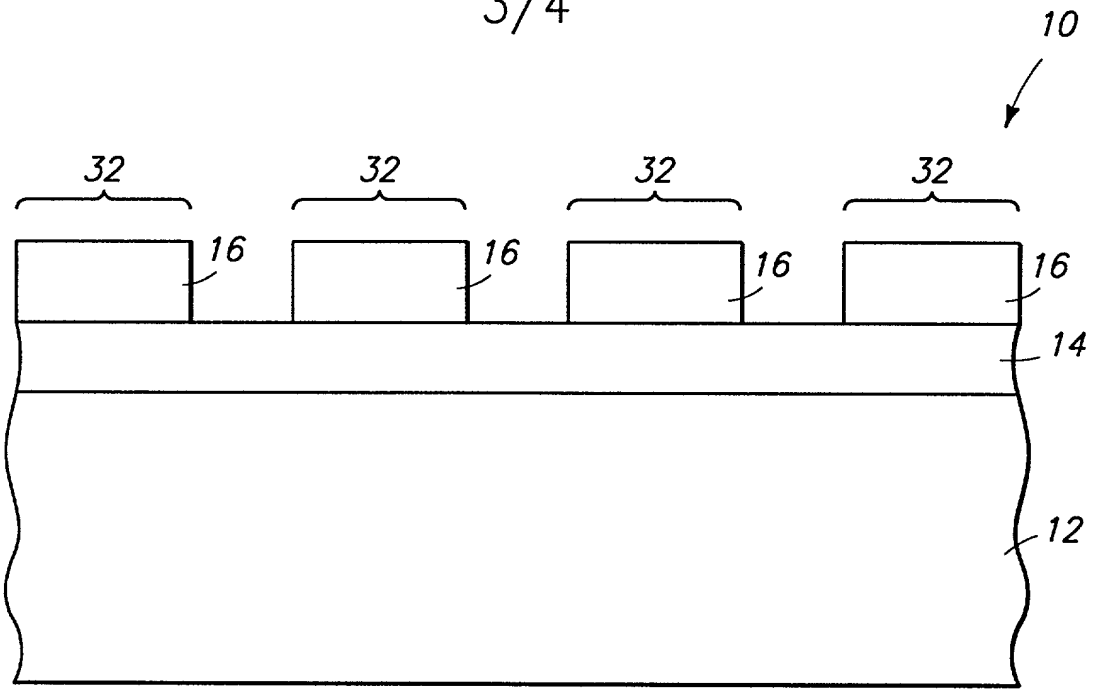
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Fig 5

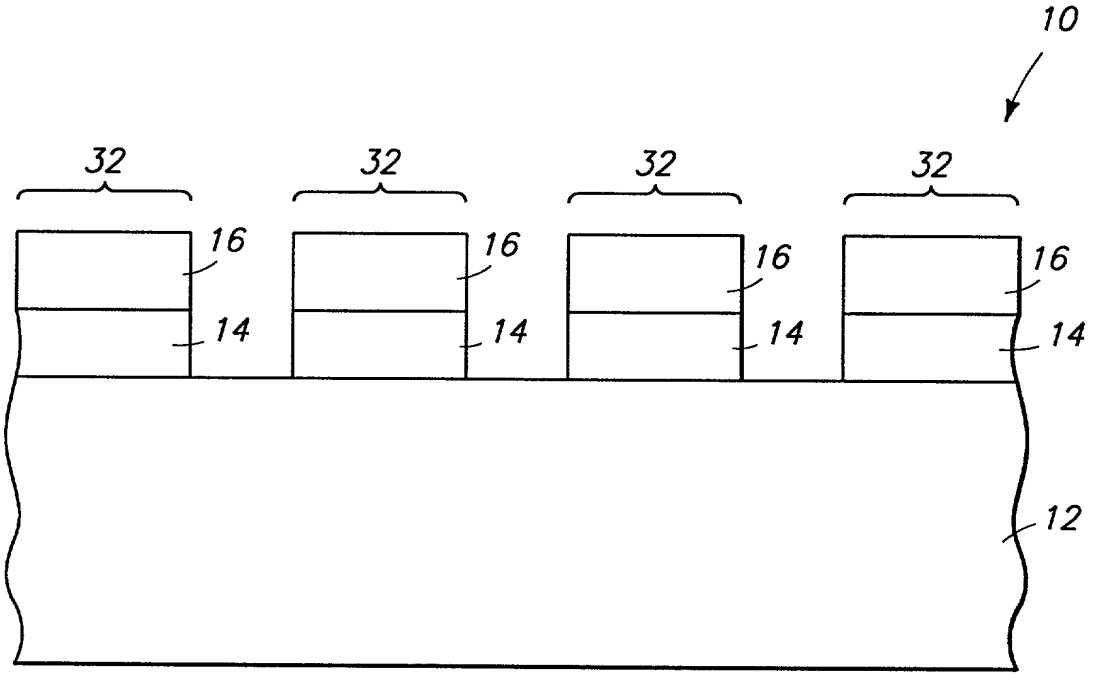
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Fig 6

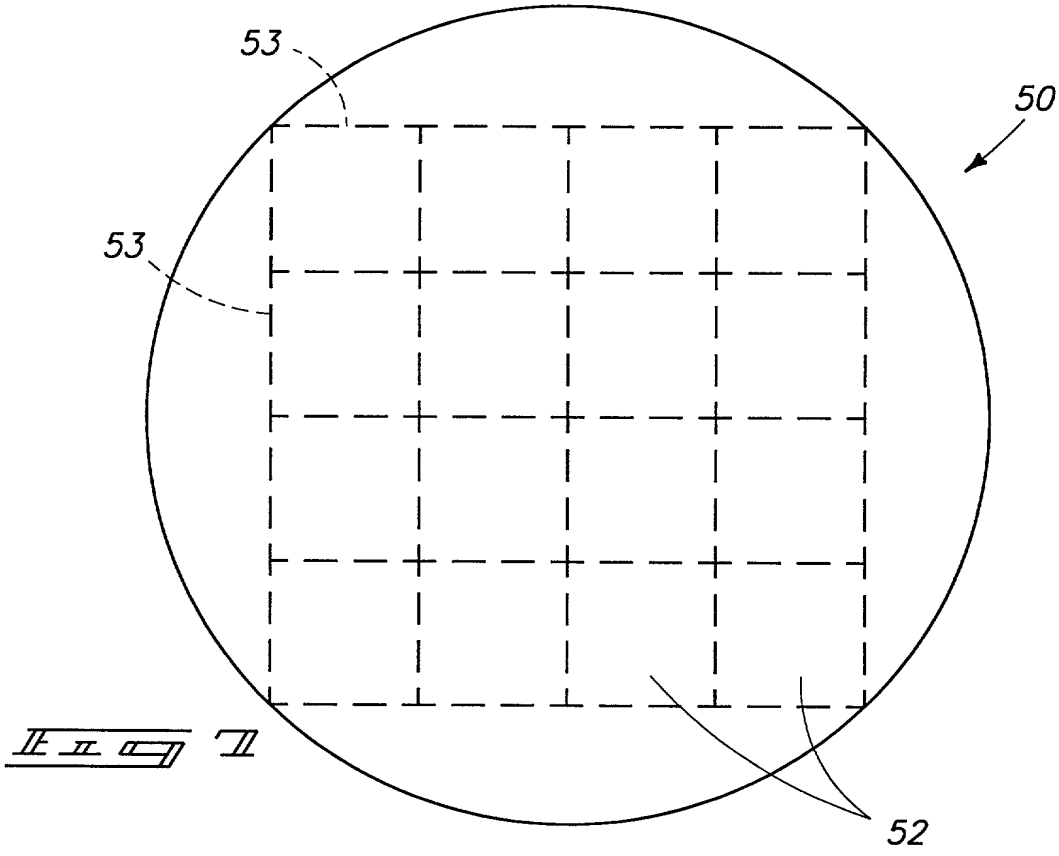

Fig. 7

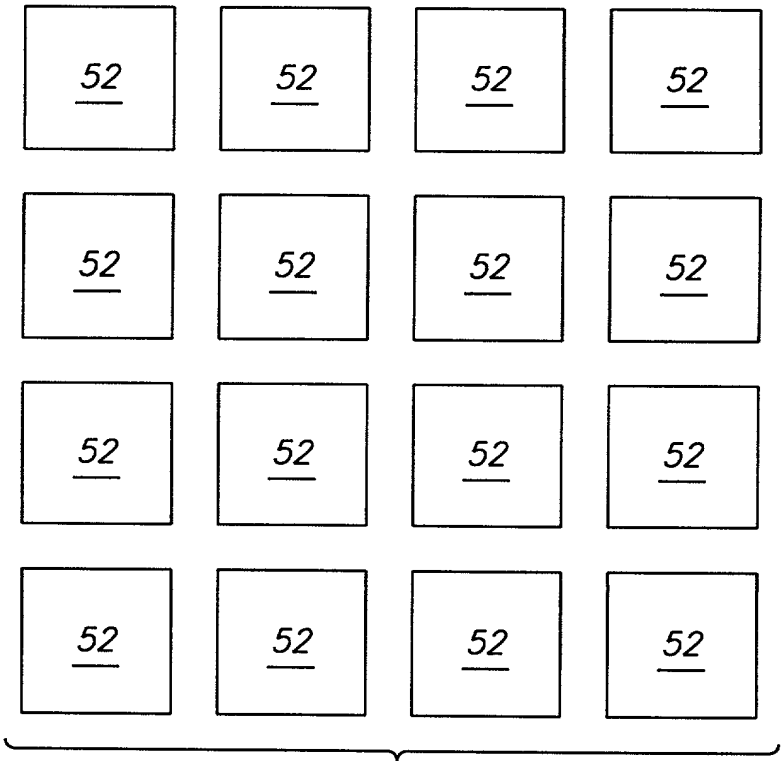

Fig. 8

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Semiconductor Processing Methods, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

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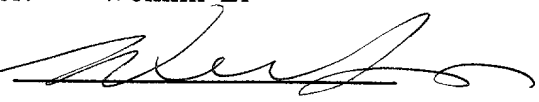
Full name of inventor: Weimin Li

Inventor's Signature: 

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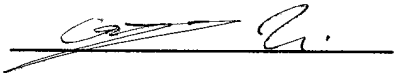
* * * * * * * * * * *

Full name of inventor: John Q. Li

Inventor's Signature: 

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